TITLE

HYSTERESIS CIRCUITS USED IN COMPARATOR

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to an electronic circuit, and particularly, to a circuit for providing hysteresis in a differential input comparator.

Description of the Related Art

A typical comparator is provided with two input terminals for comparing an input voltage signal and a reference voltage signal respectively received at the two input terminals, amplifying the voltage difference between the two signals and then producing an output signal with a logic high voltage or a logic low voltage based on the voltage difference. Generally, a logic high signal is produced at the output of the comparator when the input voltage is higher than the reference voltage. On the other hand, a logic low signal is produced at the output of the comparator when the input voltage is lower than the reference voltage.

In order to prevent erroneous changes in the output voltage of the comparator resulting from noises in the input voltage signal or in the reference voltage signal, a typical solution to provide a hysteresis circuit in the comparator, so that a threshold voltage at which the output voltage of the comparator changes from logic low to logic high is different from a threshold voltage at which the output voltage of the comparator changes from logic high to logic low. Figure 1 is a graph showing the relation between the input voltage signal and the output voltage signal of a comparator with a hysteresis characteristic, in which the

horizontal axis represents the input voltage signal Vin while the vertical axis represents the output voltage signal Vout. When the output voltage signal Vout is in a logic low state, the input voltage signal Vin must rise above an upper threshold voltage Vth so that the output voltage signal Vout will change from logic low to logic high. When the output voltage signal Vout is in a logic high state, the input voltage signal Vin must fall below a lower threshold voltage Vtl so that the output voltage signal Vout will change from logic high to logic low. The voltage difference between the upper threshold voltage Vth and the lower threshold voltage Vtl is referred to as a hysteresis width, which is usually designed to be several hundreds of Millivolts.

R.O.C. Patent Publication No. 508567, titled "Hysteresis comparing device with constant hysteresis width" discloses a comparator circuit having a hysteresis characteristic. Figure 2 illustrates a schematic circuit diagram of the hysteresis comparing device disclosed in the above patent. As shown in Figure 2, the hysteresis comparing device 20 comprises a threshold voltage generator 22, a selection switching device 24 and a comparator 26. The hysteresis comparing device 20 receives an input voltage signal Vin and produces an output voltage signal Vout. The threshold voltage generator 22 generates an upper threshold voltage Vth and a lower threshold voltage Vtl from a DC voltage signal Vdc according to a desired hysteresis width. The selection switching device 24 includes a first switch 24a and a second switch 24b, which are controlled on the basis of the output voltage signal Voutof the comparator 26 to select one of the upper threshold voltage Vth and the lower threshold voltage Vtl as a

reference voltage signal of the comparator. When the output voltage signal Vout is in a logic low state, the switch 24a is turned ON while the switch 24b is turned OFF, and thus the upper threshold voltage Vth is output from the selection switching device 24. On the other hand, when the output voltage signal Vout is in a logic high state, the switch 24a is turned OFF while the switch 24b is turned ON, and thus the lower threshold voltage Vtl is output from the selection switching device 24. According to the above design, when the output voltage signal Vout is in a logic low state, the input voltage signal Vin must rise above the upper threshold voltage Vth so that the output voltage signal Vout will change from logic low to logic high; when the output voltage signal Vout is in a logic high state, the input voltage signal Vin must fall below the lower threshold voltage Vtl so that the output voltage signal Vout will change from logic high to logic low. Thereby, the hysteresis effect is achieved.

However, the prior art circuit in Figure 2 is designed by providing an external threshold voltage generating circuit to a comparator to thereby obtain a hysteresis effect, which is disadvantageous because of its slow switching rate and the complicated circuit components. Such a comparing device is impossible to be designed into an integrated circuit. Therefore, it is desired to develop comparator hysteresis circuit, which is fast in switching rate, simple in circuit structure and suitable for application in an integrated circuit.

SUMMARY OF THE INVENTION

The object of the present invention is to provide a hysteresis circuit for a comparator, which is disposed in

the comparator circuit and has the advantages of fast switching rate, simple structure and fewer components.

Another object of the present invention is to provide a hysteresis circuit for a comparator, which is configured only by current source elements and resistor elements and thus is suitable for use in an integrated circuit to provide a hysteresis width insensible to variations of the power supply voltage and the temperature.

The hysteresis circuit according to the present invention may be employed in a differential comparator having a differential input stage including a first transistor and a second transistor. Each of the first transistor and the second transistor has a gate terminal serving as one of two input terminals of the comparator. The comparator further includes a constant current source for supplying a constant current to the differential input stage of the comparator. The hysteresis circuit of the present invention comprises a first and a second resistor elements, a first to a forth constant current source elements and a first to a forth switch elements, all disposed in the above comparator. Both the first and the second resistor elements have the same resistance value. The first resistor element is coupled between a source terminal of the first transistor and the constant current source element of the comparator, while the second resistor element is coupled between a source terminal of the second transistor and the constant current source element of the comparator. Each of the first to the forth constant current source elements produces a constant current, which is of the same value as the current produced by the constant current source of the comparator. The first switch element is coupled between the first constant current source

element and the source terminal of the first transistor so that the first constant current source element selectively supplies a constant current to the source terminal of the first transistor. The second switch element is coupled between the second constant current source element and the source terminal of the first transistor so that the second constant current source element selectively derives a constant current out from the source terminal of the first transistor. Symmetrically, the third switch element is coupled between the third constant current source element and the source terminal of the second transistor so that the third constant current source element selectively supplies a constant current to the source terminal of the second transistor. Similarly, the forth switch element is coupled between the forth constant current source element and the source terminal of the second transistor so that the forth constant current source element selectively derives a constant current out from the source terminal of the second transistor. ON/OFF operations of the first to the forth switch elements are controlled based on a signal from the output terminal of the comparator. If the signal from the output terminal of the comparator is a first logic value, then the first and the forth switch elements are turned ON while the second and the third switch elements are turned OFF. If the signal from the output terminal of the comparator is a second logic value, then the first and the forth switch elements are turned OFF while the second and the third switch element are turned ON.

With the above configuration according to the present invention, a single-side hysteresis width equal to the current value I of the constant current source element multiplied by twice the resistance value R of the resistor

element, i.e., a double-side hysteresis width equal to twice the single-side hysteresis width, can be provided.

BRIEF DESCRIPTION OF THE DRAWINGS

Objects and advantages of the present invention will be fully understood from the detailed description to follow taken in conjunction with the embodiments as illustrated in the accompanying drawings, wherein:

Figure 1 is a graph showing the changes in an output voltage of a comparator with a hysteresis characteristic;

Figure 2 depicts a schematic circuit diagram of a conventional hysteresis comparing device;

Figure 3 is a graph showing the changes in output voltage of a comparator employing the hysteresis circuit according to the present invention;

Figure 4 depicts a schematic circuit diagram of a comparator employing the hysteresis circuit according to the present invention;

Figures 5(a) and 5(b) are circuit diagrams explaining the operations of the comparator as the output signal changes from logic low to logic high; and

Figures 6(a) and 6(b) are circuit diagrams explaining the operations of the comparator as the output signal changes from logic high to logic low.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to Figure 4, a circuit diagram of a comparator employing the hysteresis circuit according to the present invention is shown. It should be noted that, for simplicity, only components associated with the hysteresis circuit, instead of complete circuit components, are illustrated in the circuit diagram in Figure 4. As shown, a differential

input comparator is provided with an input stage, including a first PMOS transistor Q1 and a second PMOS transistor Q2. The first PMOS transistor Q1 and the second PMOS transistor Q2 are two PMOS transistors with substantially the same characteristics, and the gate terminals thereof are respectively used as two input terminals of the comparator to respectively receive a first input signal Vin+ and a second input signal Vin-. The comparator further comprises a constant current source (the fifth constant current source) I5 for producing a constant current of "I", which is supplied to the input stage of the comparator. Moreover, the comparator has an output terminal (not shown) for outputting an output signal Vout, which is generated based on a voltage difference ΔV between the first input signal Vin+ and the second input signal Vin-.

According to the hysteresis circuit for a comparator of the present invention, a first resistor R1, a second resistor R2, a first constant current source I1, a second constant current source I2, a third constant current source I3, a forth constant current source I4, a first switch SW1, a second switch SW2, a third switch SW3 and a forth switch SW4 are provided in the differential input comparator. The first resistor R1 and the second resistor R2 are series coupled between a source terminal S1 of the first PMOS transistor Q1 and a source terminal S2 of the second PMOS transistor Q2. More specifically, two ends of the first resistor R1 are respectively connected to the source terminal S1 of the first PMOS transistor Q1 and to the fifth constant current source I5, and two ends of the second resistor R2 are respectively connected to the source terminal S2 of the second PMOS transistor Q2 and to the fifth constant current source I5. Both the first resistor R1 and

the second resistor R2 have substantially the same resistance value "R". Each of the first to the forth constant current sources I1~I4 produces a constant current having substantially the same current value I as the current produced by the fifth constant current source I5. The first constant current source I1 is coupled to the source terminal S1 of the first PMOS transistor Q1 via the first switch SW1 to thereby selectively supply a constant current to the source terminal S1 of the first PMOS transistor Q1 through the operation of the first switch SW1. The second constant current source I2 is coupled to the source terminal S1 of the first PMOS transistor Q1 via the second switch SW2 to thereby derive a constant current out from the source terminal S1 of the first PMOS transistor Q1 through the operation of the second switch SW2. Similarly, the third constant current source I3 is coupled to the source terminal S2 of the second PMOS transistor Q2 via the third switch SW3 to thereby supply a constant current to the source terminal S2 of the second PMOS transistor Q2 through the operation of the third switch SW3. The forth constant current source I4 is coupled to the source terminal S2 of the second PMOS transistor Q2 via the forth switch SW4 to thereby derive a constant current out from the source terminal S2 of the second PMOS transistor Q2 through the operation of the forth switch SW4. In addition, the hysteresis circuit for a comparator according to the present invention further comprises a switch element control means (not shown) for controlling the ON/OFF operations of the first to the forth switches SW1~SW4. The switch element control means controls the first to the forth switches SW1~SW4 based on the output signal Vout from the output terminal (not shown) of the comparator. If the

output signal Vout from the output terminal of the comparator is in a logic low state, the first and the forth switches are turned ON, while the second and the third switches are turned OFF. Consequently, the first constant current source I1 supplies a constant current to the source terminal S1 of the first PMOS transistor Q1, and the forth constant current source I4 derives a constant current out from the source terminal S2 of the second PMOS transistor. If the output signal Vout from the output terminal of the comparator is in a logic high state, the first and the forth switches are turned OFF, while the second and the third switches are turned ON. Consequently, the third constant current source I3 supplies a constant current to the source terminal S2 of the second PMOS transistor Q2, and the second constant current source I2 derives a constant current out from the source terminal S1 of the first PMOS transistor Q1.

The comparator employing the hysteresis circuit according to the present invention has a hysteresis characteristic as shown in Figure 3. Specifically, when the output signal Vout from the output terminal of the comparator is in a logic low state, the output signal Vout will change from logic low to logic high only if the first input signal Vin+ is higher than the second input signal Vin- plus a voltage difference of "I×2R". When the output signal Vout from the output terminal of the comparator is in a logic high state, the output signal Vout will change from logic high to logic low only if the first input signal Vin+ is lower than the second input signal Vin- minus a voltage difference of "I×2R". Depending on practical demands of the circuit design, the resistance value "R" and the current value "I" may be properly selected to obtain

a desired fixed/adjustable hysteresis width, which is insensible to variations of the power supply voltage and the temperature.

Next, the operation of the circuit according to the present invention will be described with reference to Figures 5(a), 5(b), 6(a) and 6(b).

Figures 5(a) and 5(b) are circuit diagrams explaining the operations of the comparator as the output signal changes from logic low to logic high. When the output signal Vout from the output terminal of the comparator is in a logic low state, the first and the forth switches are ON and the second and the third switches are OFF, and therefore the first constant current source I1 supplies a constant current I to the source terminal S1 of the first PMOS transistor Q1 while the forth constant current source I4 derives a constant current I out from the source terminal S2 of the second PMOS transistor Q2. At this time, if the first input signal Vin+ at the input terminal of the comparator gradually increases so that the first input signal Vin+ exceeds the second input signal Vin-, the second PMOS transistor Q2 will be turned on but the first PMOS transistor Q1 has not yet been turned off. Therefore, as shown in Figure 5(a), each the first PMOS transistor Q1 and the second PMOS transistor Q2 conducts a current of "I/2", and thus the current flowing through the first resistor R1 and the current flowing through the second resistor R2 are "I/2" and "3I/2", respectively. Accordingly, a voltage difference between the source terminal S1 of the first PMOS transistor Q1 and the source terminal S2 of the second PMOS transistor Q2 is $(I/2)\times R+(3I/2)\times R = I\times 2R$. For this reason, when the first input signal Vin+ exceeds the second input signal Vin-, the output signal Vout will not immediately

change from logic low to logic high. Instead, the output signal Vout changes from logic low to logic high only when the voltage difference ΔV between the first input signal Vin+ and the second input signal Vin- is greater than I×2R.

As shown in Figure 5(b), after the output signal Vout changes from logic low to logic high, the first and the forth switches are OFF and the second and the third switches are ON. In this case, the first and the forth constant current sources I1 and I4 are considered no longer present, and therefore the third constant current source I3 supplies a constant current I to the source terminal S2 of the second PMOS transistor Q2 while the second constant current source I2 derives a constant current I out from the source terminal S1 of the first PMOS transistor Q1. At this time, the first PMOS transistor Q1 is turned OFF, and the second PMOS transistor Q2 conducts a current of "I".

Similarly, Figures 6(a) and 6(b) are circuit diagrams explaining the operations of the comparator as the output signal changes from logic high to logic low. When the output signal Vout from the output terminal of the comparator is in a logic high state, the first and the forth switches are OFF and the second and the third switches are ON, and therefore the third constant current source I3 supplies a constant current I to the source terminal S2 of the second PMOS transistor Q2 while the second constant current source I2 derives a constant current I out from the source terminal S1 of the first PMOS transistor Q1. At this time, if the first input signal Vin+ at the input terminal of the comparator gradually decreases so that the first input signal Vin+ falls below the second input signal Vin-, the first PMOS transistor Q1 will be turned ON but the second PMOS transistor Q2 has not yet been turned OFF. Therefore,

as shown in Figure 6(a), each of the first PMOS transistor Q1 and the second PMOS transistor Q2 conducts a current of "I/2", and thus the current flowing through the second resistor R2 and the current flowing through the first resistor R1 are "I/2" and "3I/2", respectively. Accordingly, the voltage difference between the source terminal S1 of the first PMOS transistor Q1 and the source terminal S2 of the second PMOS transistor Q2 is $-(I/2)\times R-(3I/2)\times R = -I\times 2R$. For this reason, as the first input signal Vin+ falls below the second input signal Vin-, the output signal Vout will not immediately change from logic high to logic low. Instead, the output signal Vout changes from logic high to logic low only when the voltage difference ΔV between the first input signal Vin+ and the second input signal Vin- is smaller than $-I\times 2R$.

As shown in Figure 6(b), after the output signal Vout changes from logic high to logic low, the first and the forth switches are ON and the second and the third switches and OFF. In this case, the second and the third constant current sources I2 and I3 are considered no longer present, and therefore the first constant current source I1 supplies a constant current I to the source terminal S1 of the first PMOS transistor Q1 while the forth constant current source I4 derives a constant current I out from the source terminal S2 of the second PMOS transistor Q2. At this time, the second PMOS transistor Q2 is turned OFF, and the first PMOS transistor Q1 conducts a current of "I".

Although in the above embodiment of the present invention the first to the forth constant current sources I1~I4 are designed to produce the same constant current I as the fifth constant current source I5 and the first resistor R1 and the second resistor R2 are designed to have

the same resistance value R, it should be considered as illustrative and not restrictive. In other embodiments, constant current sources producing different current values and resistors having different resistance values may be employed, as long as the current values and resistance values are properly selected to obtain the hysteresis effect as described in the above embodiment.

The hysteresis circuit according to the present invention is not only suitable for differential comparison but also for single-ended comparison. For differential comparison, two input terminals Vin+ and Vin- of the comparator are respectively connected to the two signals to be compared. For single-ended comparison, the inverting input terminal Vin- of the comparator is connected to a constant DC reference voltage, and the non-inverting input terminal Vin+ of the comparator is connected to the signal to be compared. In the comparing device described with reference to Figure 2, the input at the inverting input terminal of the comparator 26 is limited by the threshold voltage generator 22, and therefore the device is not suitable for differential input comparison. In contrast to the prior art, the hysteresis circuit according to the present invention is applicable in a broad range of circuits.

While the present invention has been described with reference to the preferred embodiments thereof, it is to be understood that the invention should not be considered as limited thereby. Various modifications and changes could be conceived of by those skilled in the art without departuring from the scope of the present invention, which is indicated by the appended claims.